

# 2.5V Drive Pch MOS FET

## RTR030P02

### ●Structure

Silicon P-channel  
MOS FET

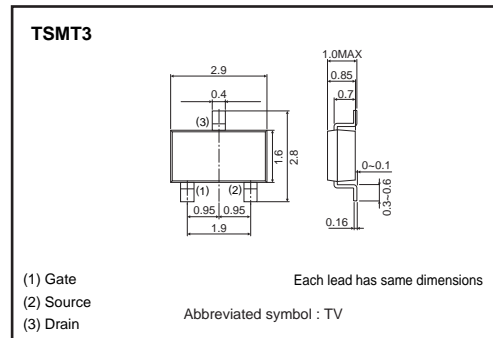
### ●Features

- 1) Low On-resistance.
- 2) Built-in G-S Protection Diode.
- 3) Small Surface Mount Package (TSMT3).

### ●Application

Power switching, DC / DC converter.

### ●External dimensions (Unit : mm)



### ●Packaging specifications

Type	Package	Taping
	Code	TL
	Basic ordering unit (pieces)	3000
RTR030P02		○

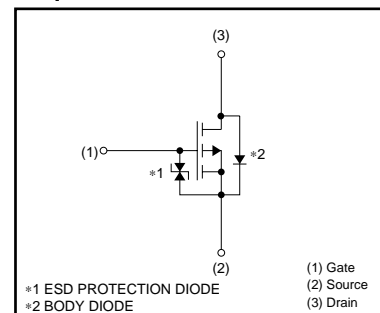
### ●Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit	
Drain-source voltage	$V_{DS}$	-20	V	
Gate-source voltage	$V_{GS}$	±12	V	
Drain current	Continuous	$I_D$	±3.0	A
	Pulsed	$I_{DP}$ *1	±12	A
Source current (Body diode)	Continuous	$I_S$	-0.8	A
	Pulsed	$I_{SP}$ *1	-3.2	A
Total power dissipation	$P_D$ *2	1.0	W	
Channel temperature	$T_{ch}$	150	°C	
Range of Storage temperature	$T_{stg}$	-55 to +150	°C	

\*1  $P_w \leq 10 \mu s$ , Duty cycle  $\leq 1\%$

\*2 Mounted on a ceramic board

### ●Equivalent circuit



### ●Thermal resistance

Parameter	Symbol	Limits	Unit
Channel to ambient	$R_{th}(ch-a)$ *	125	°C / W

\* Mounted on a ceramic board.

## Transistors

## ●Electrical characteristics (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	$I_{GSS}$	–	–	$\pm 10$	$\mu A$	$V_{GS}=\pm 12V, V_{DS}=0V$
Drain-source breakdown voltage	$V_{(BR)DSS}$	–20	–	–	V	$I_D = -1mA, V_{GS}=0V$
Zero gate voltage drain current	$I_{DSS}$	–	–	–1	$\mu A$	$V_{DS} = -20V, V_{GS}=0V$
Gate threshold voltage	$V_{GS(th)}$	–0.7	–	–2.0	V	$V_{DS} = -10V, I_D = -1mA$
Static drain-source on-state resistance	$R_{DS(on)}$ *	–	55	75	$m\Omega$	$I_D = -3.0A, V_{GS} = -4.5V$
		–	60	85	$m\Omega$	$I_D = -3.0A, V_{GS} = -4.0V$
		–	90	125	$m\Omega$	$I_D = -1.5A, V_{GS} = -2.5V$
Forward transfer admittance	$ Y_{fs} $ *	2.5	–	–	S	$V_{DS} = -10V, I_D = -1.5A$
Input capacitance	$C_{iss}$	–	840	–	pF	$V_{DS} = -10V$
Output capacitance	$C_{oss}$	–	140	–	pF	$V_{GS}=0V$
Reverse transfer capacitance	$C_{rss}$	–	100	–	pF	$f=1MHz$
Turn-on delay time	$t_{d(on)}$ *	–	12	–	ns	$I_D = -1.5A$
Rise time	$t_r$ *	–	20	–	ns	$V_{DD} = -15V$
Turn-off delay time	$t_{d(off)}$ *	–	50	–	ns	$V_{GS} = -4.5V$
Fall time	$t_f$ *	–	20	–	ns	$R_L=10\Omega$
Total gate charge	$Q_g$	–	9.3	–	nC	$V_{DD} = -15V$
Gate-source charge	$Q_{gs}$	–	1.6	–	nC	$V_{GS} = -4.5V$
Gate-drain charge	$Q_{gd}$	–	2.6	–	nC	$I_D = -3.0A$

\*Pulsed

## ●Body diode characteristics (Source-drain) (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	$V_{SD}$	–	–	–1.2	V	$I_S = -0.8A, V_{GS}=0V$

Transistors

●Electrical characteristic curves

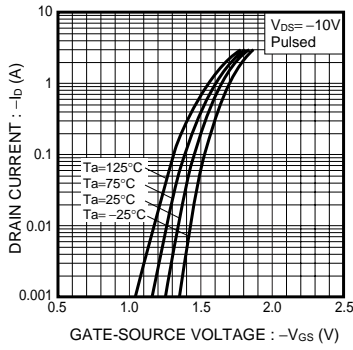


Fig.1 Typical Transfer Characteristics

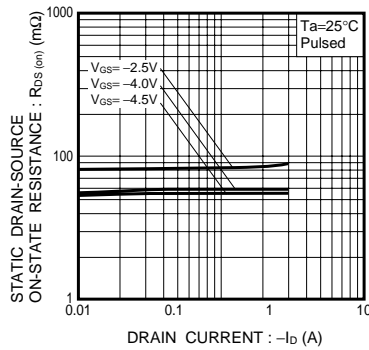


Fig.2 Static Drain-Source On-State Resistance vs. Drain Current

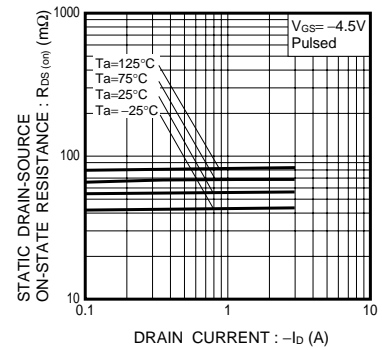


Fig.3 Static Drain-Source On-State Resistance vs. Drain Current

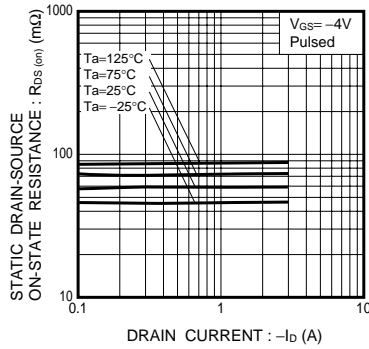


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current

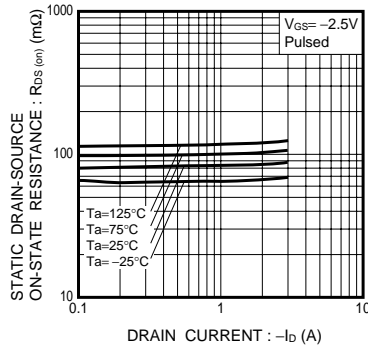


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current

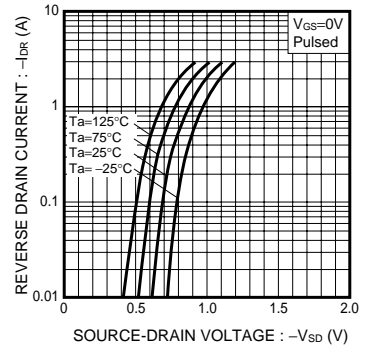


Fig.6 Reverse Drain Current vs. Source-Drain Voltage

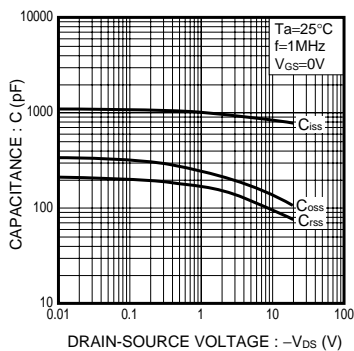


Fig.7 Typical Capacitance vs. Drain-Source Voltage

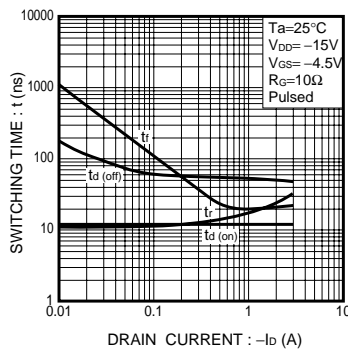


Fig.8 Switching Characteristics

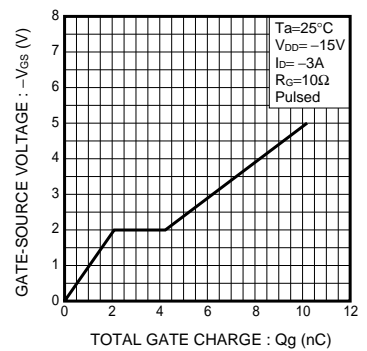


Fig.9 Dynamic Input Characteristics

Transistors

●Measurement circuits

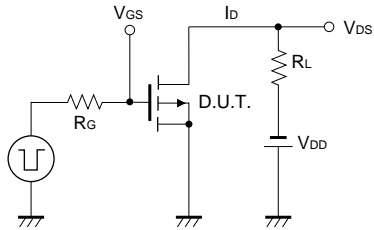


Fig.10 Switching Time Test Circuit

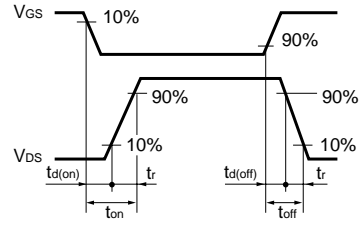


Fig.11 Switching Time Waveforms

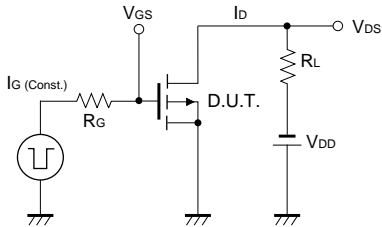


Fig.12 Gate Charge Test Circuit

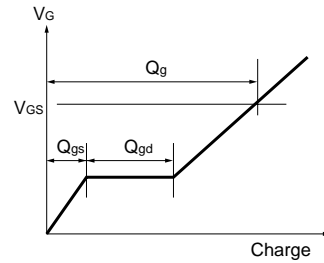


Fig.13 Gate Charge Waveform

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